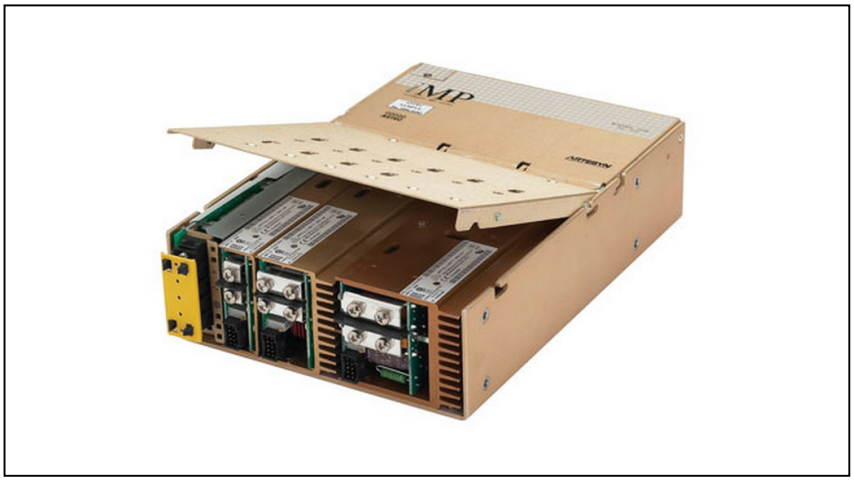
iMP Series

I2C Clock Stretching and Timeout



Technical Reference Summary*

This Technical Reference Note describes the I2C Clock Stretching and Timeout of iMP series.

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1. When I2C Master Does Not Support Clock Stretching

Background information on clock stretching

There are two types of I2C slave device clock stretching, inter-bit and inter-byte.

Inter-bit clock stretching is the extension of clock low period per bit clock pulse within a byte. This is commonly present on slow I2C devices and is used to be able to synchronize with a device capable of higher speed. The iMP PSU does not do inter-bit clock stretching since it can support up to 100KHz operating frequency.

Inter-byte clock stretching is the extension of clock low period after a byte has been received or transmitted. This is a provision for the slave device to process the received data or perform other system critical tasks before releasing the clock line again. When the slave releases the clock, it indicates that it is ready to receive or transmit one more byte. The iMP PSU makes use of inter-byte clock stretching

The iMP cases (iMP4, iMP8, and iMP1)has two signal connectors located in the front panel, J1 – PFC Input Connector and J2 – I2C Bus Output Connector, and two LEDs which serve as visual status indicators.

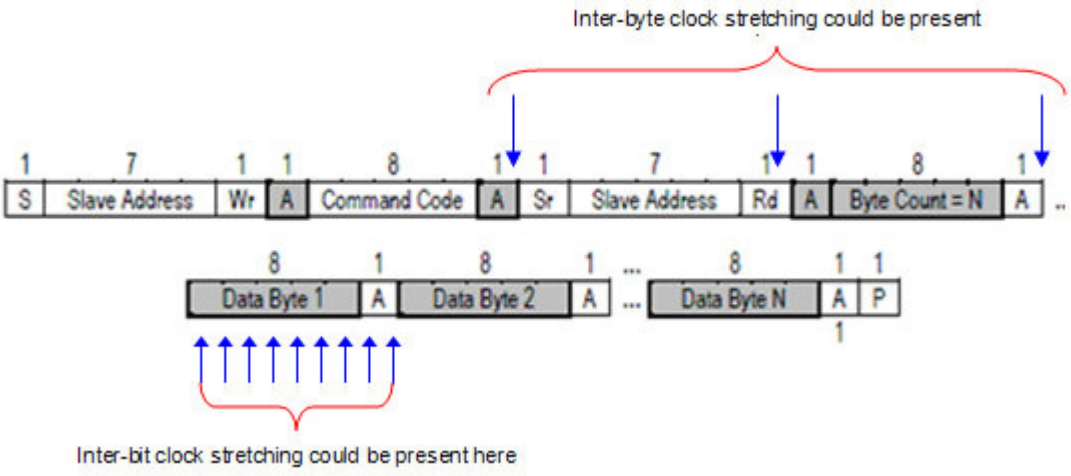

Figure 1. Sample illustration

These conditions are seamless for I2C master devices that inherently support clock stretching. **If clock stretching is not supported**, the succeeding sections describe I2C transaction delay recommendations to avoid communication errors.

Recommended Delay for Clock Stretching

Insert a 330usec inter-byte delay.

Sample Transaction

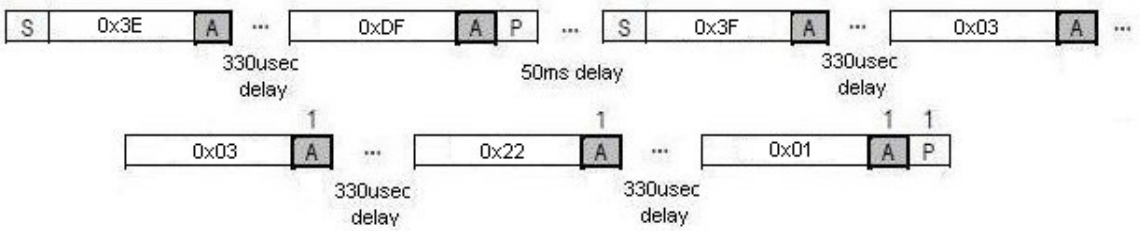

Figure 2. Transaction with 330usec delay between bytes

2. Delay between transactions

Background information on transaction delay

There are internal processing performed by the PSU firmware after an I2C transaction. This is common behavior after write transactions, wherein the data written in a command code may be required to be processed first before being able to respond correctly to another transaction.

Recommended Delay for Clock Stretching

Insert a 50msec delay between transactions.

Sample Transaction

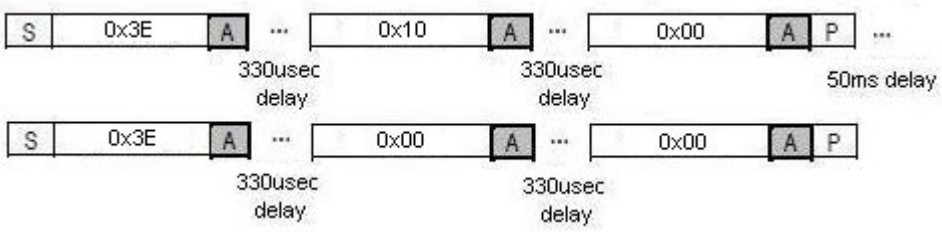

Figure 3. 50msec delay in between transactions

3. Timeout

The implemented I2C timeout in iMP is 37ms from the start bit. The timeout timer will start when it detects a start condition. If the duration of transaction exceeds this value, the I2C will reset. Any on-going transaction during the I2C reset will not be completed properly.

The PSU I2C will be able to respond to clock frequencies less than 10KHz. However, the timeout period will be the limiting factor.

If the master is operating at 5KHz and if a 330usec delay is inserted between bytes, there is only a maximum of 17 bytes (including address bytes) that can be used within an I2C START and STOP condition.

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