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# PRODUCT CHANGE NOTICE FORM

PCN NO. 0012
DATE: 14 July 2016

CUSTOMER: Standard Product
CUSTOMER P/N: DS1600SPE-3 & -001

FAX NO:
VENDOR P/N: DS1600SPE-3 & -001

TEL. NO:
POWER SUPPLY WATTAGE: 1600W

ORIGINATOR ENGINEER: Jon Karlo Lee
CHECKED BY: Louie Cuevas
APPROVED BY: Louie Cuevas
FORWARD TO NAME: Richard Daniel Caubang

DEPARTMENT: Team 1
RESPONSIBLE ENGINEER: Jon Karlo Lee
PRIORITY: [ ] EMERGENCY [X] URGENT [ ] ROUTINE
IMPACT [ ] NO COST [ ] COST AMOUNT [ ] SCHEDULE

TYPE OF REQUEST:
[ ] PROCESS CHANGE [X] DESIGN CHANGE [ ] QUALITY [ ] RELIABILITY [ ] COMPONENT APPLICATION [ ] SAFETY
[ ] SECOND SOURCE [ ] OTHERS:

ACCOMPANYING MATERIAL:
[ ] CUSTOMER SPEC [ ] ARTWORK [ ] SOURCE LIST [ ] TEST PLAN [ ] COMPONENTS/UNITS
[ ] DRAWING [X] TEST DATA [ ] B.O.M. [ ] COMPONENT SPECS [ ] SCHEMATIC
[ ] FRU Specs [ ] PSMI Compliance Specs Other [] OTHERS:
REQUESTED DATE OF COMPLETION: AS SOON AS POSSIBLE
CUSTOMER BUYER AFFECTED:

| DESCRIPTION OF REQUEST | JUSTIFICATION |
|---|---|
| • Change control board resistors R410, R411 to 8.45kΩ (IPN: 301-011706-8451). Main Board resistors R4, R16 to 49.9Ω (301-011707-49R9).<br>• Update secondary firmware i2c glitch filter. (IPN: 630-002422-0013, FW v04.10.00)<br>• Update Installation and Operating Instruction. (IPN: 970-010755-0001) | • Improve I2C communication noise rejection, error rate especially at SDA/SCL rise times >650ns<br>• Update Operating Instruction, change rating (from 100-140Vac to 100-127Vac) and update into new OI format |

Model Revision References:

1. **DS1600SPE-3** Rev CY to CZ
   EEPROM register 9Bh was CY is CZ

2. **DS1600SPE-3-001** Rev BX to BY
   EEPROM register 9Bh was BX is BY

ASTEC SAFETY CERTIFICATE: _____

APPROVALS:
CUSTOMER ENGINEER RESPONSE: _____

SIGNATURE: Richard Daniel Caubang _____ DATE: 7/21/2016

CUT IN DATE: Immediate Implementation
SERIAL NUMBER:

ASTEC-PHIL-PCN-2004-001

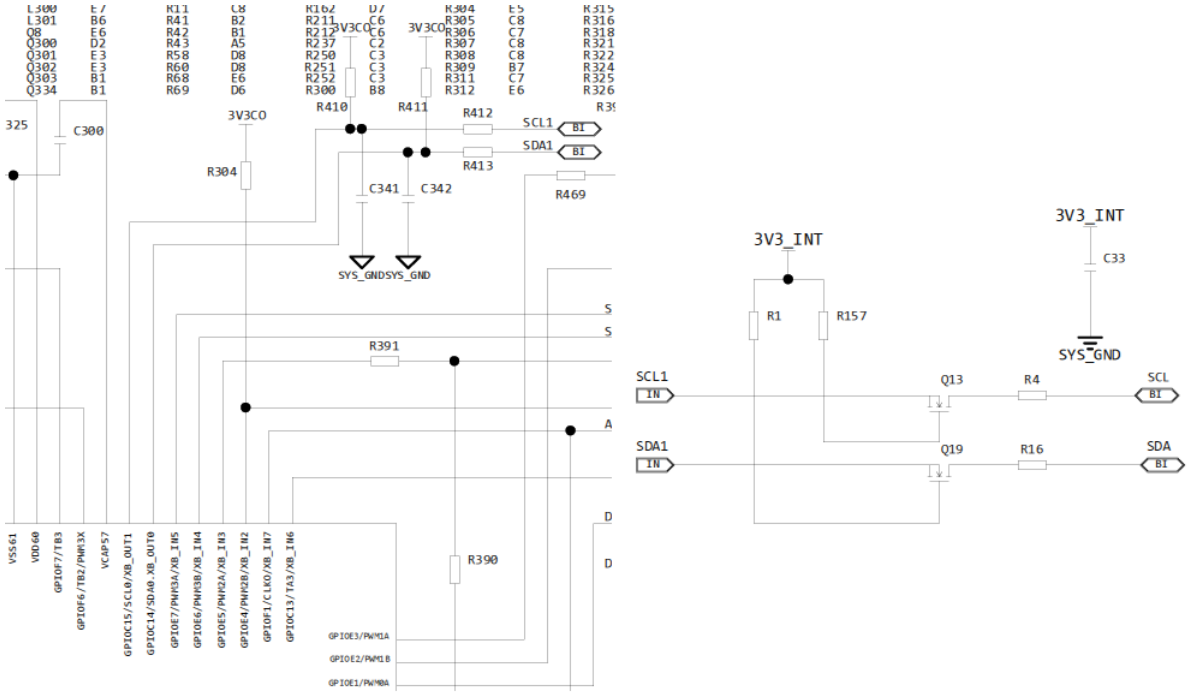
**Objective:**

- Improve I2C communication error rate especially at slower rise times (>650ns).
- To have no I2C communication errors as per I2C SMBUS v2.0 standard.

**Background:**

When the PSU was tested with an effective rise-time of 1usec, the I2C communication was not always successful. When the pull-up was changed to reduce the rise-time down to about 650nsec, the error rates were reduced.

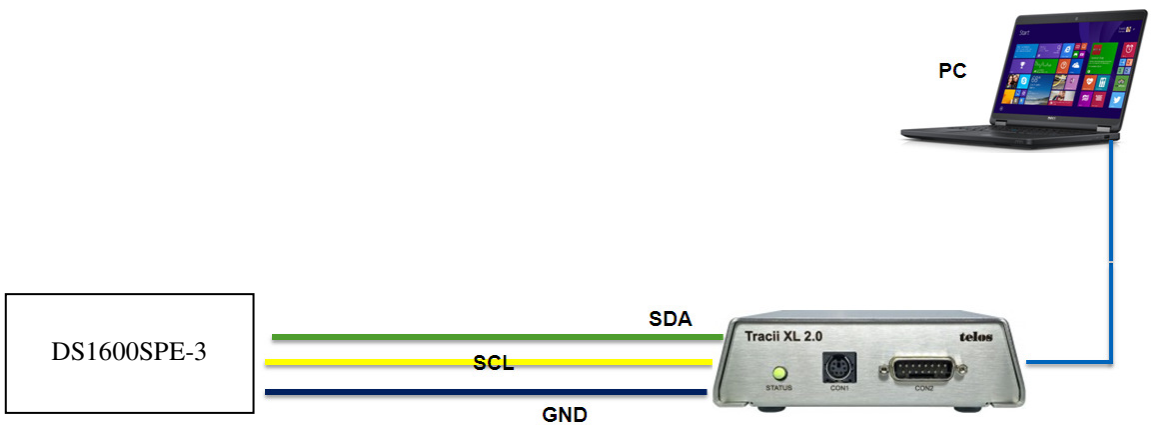
Schematic of SDA/SCL lines inside PSU:



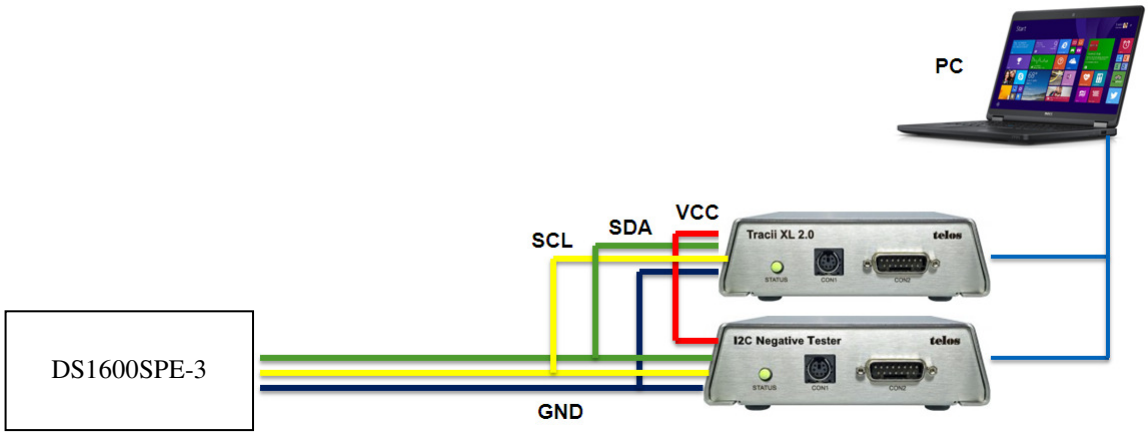

**Test method:**

To properly check and verify I2C communication, Telos I2C Studio was used:

A. Use Telos Master Tracii XL 2.0 to check error rate during communication burn-in test



B. Use Telos I2C Negative Tester for negative testing

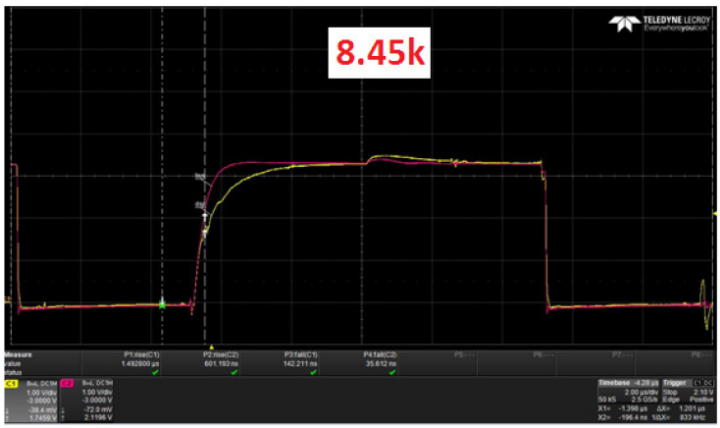



**Test Results:**

***A. Optimizing internal pull-up value: R410 and R411 to 8.45kohm***

- Waveform comparison using 8.45k internal pull-up:

Ch1 (yellow) = DSP pin, SDA
Ch2 (red) = Load side, SDA




- Error Rate at 8.45k internal pull-up:

| Rise time (0.65V~2.25V) | 8.45kΩ change |
|---|---|
| | Error Rate |
| 950ns | 1002/10777 = 9.29% |
| 750ns | 58/10706 = 0.542% |
| 650ns | 0/10308 = 0.0% |
| 550ns | 0/10501 = 0.0% |

***B. Adjusting digital noise glitch filter with optimized internal pull-up resistors R410, R411:***

- No I2C errors after changing internal SDA/SCL pull-up (from 39k to 8.45k) with modified digital glitch filter (from 4 to 12 cycles). After changing glitch filter, was able achieve no error even at ~1us rise time.

  Test results table with rise time (0.65V to 2.25V, SMBUS ver2) at ~1usec,

| PSU condition | Error Rate |
|---|---|
| 90Vac, NL | 0 of 127,194 |
| 90Vac, FL | 0 of 110,562 |
| 264 Vac, NL | 0 of 240,382 |
| 264 Vac, FL | 0 of 227,652 |

- Digital glitch filter was also tested at 4, 8, 12 and 15. No errors at filter = 12. At filter = 15, there occasional errors.

***C. Review possible solution to address I2C communication errors via SW change only.***

- Changing SW for glitch filter will still have 0.003% error rate at 1us rise times.
- HW and SW change have no errors.

## SW only

| Condition A: Loading board pull-up at 800Ω | |
|---|---|
| PSU condition | Error rate |
| 230Vac, NL | 0 of 100,000 |
| 230Vac, FL | 3 of 100,000 |

| Condition B: Risetime at <1us | |
|---|---|
| PSU condition | Error rate |
| 230Vac, NL | 0 of 100,000 |
| 230Vac, FL | 26 of 100,000 |

## HW and SW

| Condition A: Loading board pull-up at 800Ω | |
|---|---|
| PSU condition | Error rate |
| 230Vac, NL | 0 of 100,000 |
| 230Vac, FL | 0 of 100,000 |

| Condition B: Risetime at <1us | |
|---|---|
| PSU condition | Error rate |
| 230Vac, NL | 0 of 100,000 |
| 230Vac, FL | 0 of 100,000 |

- *Test communication using different bus pull-up resistors to check response at different rise times*

# Master Termination

Test > Master Termination

## *Setup*

| Negative Tester | |
|---|---|
| Level Thresholds | 30 / 70 % |
| **Tracer** | |
| Level Thresholds | 30 / 70 % |
| **Test Configuration** | |
| I2C Address (Tested Slave) | 0x59 (7 bit) |

## *Results*

| Direction | Termination (Ohm) | Input Pattern (SVG) | Trace Data (HTML) | ADC Data (SVG) | Trace/ADC Data (I2CL) | Result |
|---|---|---|---|---|---|---|
| RX | 429 | X | X | X | X | Ok |
| RX | 461 | X | X | X | X | Ok |
| RX | 534 | X | X | X | X | Ok |
| RX | 595 | X | X | X | X | Ok |
| RX | 656 | X | X | X | X | Ok |
| RX | 710 | X | X | X | X | Ok |
| RX | 762 | X | X | X | X | Ok |
| RX | 900 | X | X | X | X | Ok |
| RX | 1058 | X | X | X | X | Ok |
| RX | 1217 | X | X | X | X | Ok |
| RX | 1376 | X | X | X | X | Ok |
| RX | 1534 | X | X | X | X | Ok |
| RX | 1693 | X | X | X | X | Ok |
| RX | 1852 | X | X | X | X | Ok |
| RX | 2011 | X | X | X | X | Ok |
| RX | 2169 | X | X | X | X | Ok |
| RX | 2328 | X | X | X | X | Ok |
| RX | 2487 | X | X | X | X | Ok |
| RX | 2646 | X | X | X | X | Ok |
| RX | 2804 | X | X | X | X | Ok |
| RX | 2963 | X | X | X | X | Ok |
| RX | 3122 | X | X | X | X | Ok |
| RX | 3280 | X | X | X | X | Ok |
| RX | 3439 | X | X | X | X | Ok |
| RX | 3598 | X | X | X | X | Ok |
| RX | 3757 | X | X | X | X | Ok |
| RX | 3915 | X | X | X | X | Ok |
| RX | 4074 | X | X | X | X | Ok |
| RX | 4233 | X | X | X | X | Ok |
| RX | 4392 | X | X | X | X | Ok |
| RX | 4550 | X | X | X | X | Ok |
| RX | 4709 | X | X | X | X | Ok |
| RX | 4868 | X | X | X | X | Ok |
| RX | 5026 | X | X | X | X | Ok |
| RX | 5185 | X | X | X | X | Ok |
| RX | 5344 | X | X | X | X | Ok |
| RX | 5503 | X | X | X | X | Ok |
| RX | 5661 | X | X | X | X | Ok |
| RX | 5820 | X | X | X | X | Ok |
| RX | 5979 | X | X | X | X | Ok |
| RX | 6138 | X | X | X | X | Ok |
| RX | 6296 | X | X | X | X | Ok |

| | | | | | | |
|---|---|---|---|---|---|---|
| RX | 6455 | X | X | X | X | Ok |
| RX | 6614 | X | X | X | X | Ok |
| RX | 6773 | X | X | X | X | Ok |
| RX | 6931 | X | X | X | X | Ok |
| RX | 7090 | X | X | X | X | Ok |
| RX | 7249 | X | X | X | X | Ok |
| RX | 7407 | X | X | X | X | Ok |
| RX | 7566 | X | X | X | X | Ok |
| RX | 7725 | X | X | X | X | Ok |
| RX | 7884 | X | X | X | X | Ok |
| RX | 8042 | X | X | X | X | Ok |
| RX | 8201 | X | X | X | X | Ok |
| RX | 8360 | X | X | X | X | Ok |
| RX | 8519 | X | X | X | X | Ok |
| RX | 8677 | X | X | X | X | Ok |
| RX | 8836 | X | X | X | X | Ok |
| RX | 8995 | X | X | X | X | Ok |
| RX | 9153 | X | X | X | X | Ok |
| RX | 9312 | X | X | X | X | Ok |
| RX | 9471 | X | X | X | X | Ok |
| RX | 9630 | X | X | X | X | Ok |
| RX | 9788 | X | X | X | X | Ok |
| RX | 9947 | X | X | X | X | Ok |
| RX | 10106 | X | X | X | X | Ok |
| RX | 10265 | X | X | X | X | Ok |
| RX | 10423 | X | X | X | X | Ok |
| RX | 10582 | X | X | X | X | Ok |
| RX | 10741 | X | X | X | X | Ok |
| RX | 10900 | X | X | X | X | Ok |

With below changes, DS1600SPE-3 was able to pass communicate at different pull-up resistors ranging from 429Ω to 10900Ω. This test has effectively swept the entire rise time conditions.

Other tests that was performed and passed I2C negative tester:

- Master clock diversifying
- Master data
- Master speed
- Master stop
- Master stress
- Master termination
- Master timing

Conclusion:

Systems with I2C bus rise times of less than 650ns are not going to be affected by this change. As I2C communications below 650ns rise times have no or minimal errors during prolonged communication burn-in tests.

For systems with I2C bus rise times greater than 650ns, below changes are needed to effectively reduce error rates to zero:

- Internal SDA/SCL pull-up R410 and R411 to 8.45kΩ
- Secondary firmware with modified digital glitch filters (from 4 to 12 cycles).

These changes were tested at maximum I2C standard rise time of 1us with no errors after more than 1 hour of continuous communication at 100 kHz speed, 15ms polling rate.

With all the changes stated above, the DS1600SPE-3 has passed all communication tests on a sample system.